REMARKS

Claims 1-19 are all the claims presently pending in the application. Claim 19 has been amended to more particularly define the invention. Claims 3-19 have been withdrawn from prosecution. Of the remaining claims, claim 1 is independent.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**" These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, that Applicant's intent is to encompass equivalents of all claim elements.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Houlihan, et al. (U.S. Patent No. 6,258,673 B1) in view of Huang, et al. (U.S. Patent No. 6,037,222).

This rejection is respectfully traversed in the following discussion.

I. THE RESTRICTION REQUIREMENT

Firstly, the Office Action withdraws claims 3-19 from prosecution as allegedly being directed to an invention which is independent or distinct from the invention which was originally claimed because: "claims 3-19 could be made by a process materially different from those/that of claims 1-2."

Applicants respectfully traverse this election of species.

Applicants respectfully submit that the subject matter of all claims 1-19 is sufficiently related that a thorough search for the subject matter of any one group of claims would necessarily encompass a search for the subject matter of the remaining claims. Thus, Applicants respectfully submit that the search and examination of the entire application could be performed without serious burden.

M.P.E.P. § 803 clearly states that "if the search and examination of the entire application can be made without serious burden, the Examiner must examine it on its merits, even though it includes claims to distinct or independent inventions" (emphasis added). Applicants respectfully submit that the Examiner has clearly failed to provide a prima facie showing of a serious burden by failing to provide "by appropriate explanation of separate classification, or separate status in the art, or a different field of search" (M.P.E.P. § 803).

Applicants respectfully submit that the policy requiring examination of an entire application even though it may include distinct inventions, should be applied in the present application in order to avoid unnecessary delay and expense to Applicants and duplicative examination by the Patent Office. Applicants respectfully request reconsideration and

withdrawal of the restriction requirement and to examine all claims in this application.

Secondly, the Examiner appears to base authority to automatically withdraw claims from examination by asserting that claims 3-19 were "non-elected" because a different invention "has been constructively elected by original presentation for prosecution on the merits." However, Applicants note that the invention recited in claims 3-19 was also "elected by original presentation." The Examiner appears to assert that claims 1 and 2, being directed to a product, and claims 3-19, being directed to a process for making that product, are distinct. Applicant respectfully points out to the Examiner that claims 3-17 as originally presented are, and have always been, directed to a process of making the product of claim 1. Therefore, Applicant respectfully submits that the Examiner cannot *sua sponte* withdraw claims 3-19 from examination based upon the false assertion that this invention was not originally presented and Applicant respectfully request withdrawal of this restriction requirement.

Lastly, in view of the fact that the process of making the product recited in claims 3-17 have already been searched and examined as evidenced by the Office Action issued on February 27, 2002, there can be no serious burden to examine these claims. This invention has already been examined. Therefore, any assertion that would be any additional serious burden by the Examiner would be blatantly false. Applicants respectfully request withdrawal of the restriction requirement.

In spite of the fact that the Examiner did not have the authority to withdraw claims as being directed to a "constructive" non-election and the lack of any serious burden on the Examiner, should the Examiner decide to maintain this requirement, Applicants elect the species of claims 1 and 2 with traverse.

Applicants also reserve the right to rejoinder of withdrawn claims 3-19 pursuant to M.P.E.P. § 821.04 after claims 1-2 are indicated as being allowable.

II. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device which includes a semiconductor device comprising a first MOSFET, a second MOSFET and a third MOSFET. The first MOSFET has a relatively low threshold level and a first gate oxide film. The second MOSFET is an n-type with a relatively higher threshold level and a second gate oxide which is thicker than the first gate oxide film. The third MOSFET is a p-type with a relatively higher threshold level and a third gate oxide film that is thicker than the first gate oxide film and thinner than the second gate oxide film. Implantation treatments of fluoride ions in the regions of the high threshold level MOSFETs are performed before forming the gate oxide films. The fluoride ions encourage the oxidation of the gate oxide films. Each implantation is different for the high threshold level MOSFETs.

The present invention is also directed to a method for fabricating a semiconductor device on a semiconductor substrate. The method includes forming an isolation region within a semiconductor substrate and close to a surface of the semiconductor substrate to define a first region for a first gate oxide film of a first MOSFET and a second region for second and third MOSFETs. The method also includes selectively implanting fluorine ions into a first part of the second region with a first ion-implantation condition. The first part of the second region is for

the second MOSFET. The first ion-implantation condition is determined to form a second gate oxide film. The method also includes selectively implanting fluorine ions into a second part of the second region with a second ion-implantation condition. The second part of the second region is for the third MOSFET. The second ion-implantation condition is determined to form a third gate oxide film. The method also includes simultaneously growing oxide films on and over the first and second regions of the semiconductor substrate and forming the first to third MOSFETs by using the simultaneously grown oxide films, so that the first to third MOSFETs have the first to third gate oxide films, respectively. The second gate oxide film is thicker than the first gate oxide film and the third gate oxide film is thicker than the first gate oxide film and is thinner than the second gate oxide film. Additionally, the threshold level of the first MOSFET is relatively low and the threshold levels of the second and third MOSFETs are relatively high, and the second MOSFET is an n-type and the third MOSFET is a p-type.

Conventional processes for fabricating semiconductor devices with MOSFETs having different threshold levels use selective implantation of fluorine ions to provide gate oxide films having different thicknesses. However, these methods have never been applied to CMOS circuit fabrication which takes into consideration the properties of n-type and p-type MOSFETs.

By contrast, the present invention is a configuration and method which provides a CMOS semiconductor structure which can achieve high speed operation, high reliability and low consumption power using suitable gate oxide film thicknesses. This is a non-trivial matter because, as the inventors discovered, n-type and p-type MOSFETs operating with the same threshold level have gate-channel leakage current characteristics which are different from each

other. Thus, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET does not need to be equal to that of the n-type MOSFET. To the contrary, the inventors discovered that the thickness of the gate oxide film of the p-type MOSFET may be thinner than that of the complimentary n-type MOSFET because the leakage current of the p-type MOSFET is one order of magnitude smaller than that of the n-type MOSFET. Additionally, the thinner gate oxide film of the p-type MOSFET increases the operating speed.

III. THE PRIOR ART REFERENCES

The Examiner alleges that Huang et al. would have been combined with Houlihan et al. to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Firstly, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to different matters. Specifically, the Houlihan et al. reference is directed to avoiding the pitfalls of a first conventional method of requiring multiple HF etches (col. 1, lines 18-25) and a second conventional method of relying solely upon nitrogen implantation (col. 1, lines 26-32) to provide different gate oxide film thicknesses for generic transistors by combining aspects of each of these conventional methods (col. 2, lines 11-57), whereas the Huang et al. reference is specifically directed to providing a thin gate oxide for FETs on logic areas of a substrate and thick gate oxide layers on memory regions for an embedded logic device (col. 2, lines 31-35) by forming a 1st thin gate oxide layer 20 over

the entire device, etching away portions of the 1st thin gate oxide layer 20 in the memory region 14, forming a 2nd thick gate oxide 34 over the entire device, and lastly, etching the 2nd thick gate oxide 34 from the logic areas 12. Clearly, the method of providing for different gate oxide thicknesses through multiple etching processes which is taught by Huang et al. is exactly the type of multiple etchings that Houlihan et al. explains as having undesireable side affects (col. 1, lines 21-25). Houlihan et al. explains that the type of multiple etchings disclosed by Huang et al. is exactly the method that Houlihan et al. is trying to avoid. In other words, Houlihan et al. teaches away from the method of Huang et al. Thus, one of ordinary skill in the art would not have been motivated to modify the teachings of Houlihan et al. of providing different thicknesses for gate oxide films by going back to the conventional method of multiple etching processes as taught by Huang et al.

Secondly, even assuming arguendo, that one of ordinary skill in the art would have been motivated to combine these references, even if combined, the combination would not teach or suggest each and every element of the claimed invention.

The Houlihan et al. reference discloses a method of forming an integrated circuit having four thicknesses of gate oxide in four sets of active areas (Abstract). The Houlihan et al. reference is concerned with the problem of providing transistors having different characteristics through providing different gate oxide films having different thicknesses. The Houlihan et al. reference explains that conventional methods for providing different gate oxide thicknesses is by providing a resist on areas of gate oxide upon which a thicker gate oxide film is desired and repeatedly etching the remaining areas (col. 1, lines 14-25). The Houlihan et al. reference

explains that this method causes problems by creating edge "divots" and planar recess in shallow trench isolation areas (col. 1, lines 21-25).

Houlihan et al. also explains that there is a method for providing several different thicknesses of gate oxide films by using nitrogen implantation (col. 1, lines 26-27). However, Houlihan et al. teaches that this implantation is disadvantageous because the gate thicknesses are dependent upon the nitrogen implant dose and that high dosages can degrade gate oxide film reliability.

Houlihan et al. attempts to address these problems by teaching a method whereby a blanket oxide 20 is formed on active areas (100, 200, 300 and 400). A mask 30 is provided and the blanket oxide 20 in active areas 100 and 400 are exposed to nitrogen implantation (Fig. 2). The reference explains that the nitrogen implantation slows the oxidation process. Next, the mask 30 is removed and an etching mask 40 is formed over active areas 300 and 400. The blanket oxide 20 in active areas 100 and 200 is then etched away through a single HF dip. Lastly, the etching mask 40 is removed and the entire device is thermally oxidized. The resulting device provides gate oxide films with increasing levels of thickness from 100 to 400, respectively.

Contrary to the assertion of the Examiner, Houlihan et al. does not teach or suggest the features of independent claim 1 including a MOSFET of n-type conductivity. Rather, Houlihan et al. merely refers generically to "active areas" 100, 200, 300 and 400 (col. 2, line 8; col. 3, lines 37-38). Houlihan et al. does not teach or suggest a MOSFET of n-type conductivity.

Indeed, the Office Action admits that Houlihan et al. does not teach or suggest the features of independent claim 1 including a MOSFET of p-type conductivity.

Contrary to the assertions of the Examiner, Huang et al. does not remedy the deficiencies of Houlihan et al. Rather, Huang et al. is directed to providing a thin gate oxide layer for all FETs on logic areas of a substrate while simultaneously providing a thick gate oxide layer for all FETs on memory regions. Huang et al. only discloses providing different gate oxide thicknesses among varying regions of an entire semiconductor device. Huang et al. does not disclose an n-type MOSFET having a gate oxide film thicker than a first gate oxide film and a p-type MOSFET having a gate oxide film which is thicker than the first gate oxide film and thinner than the second gate oxide film. Rather, Huang et al. only discloses grouping generic MOSFETs together based upon their region and not based upon their type. Applicants respectfully request withdrawal of this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-19, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 11/14/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

The claims were amended as follows:

19. (Amended) The method of claim 18, wherein the standby current in each of the second and third MOSFETs [do not depend] depends on [the gate-channel leakage current characterisics but] on [the] subthreshold characteristics, said subthreshold characteristics comprising other than gate channel leaking current characteristics.